REMARKS/ARGUMENTS

The Examiner states that claims 1-19 are presented for examination. The Examiner states claims 6-10 and 16-19 are withdrawn from further consideration by the amendment filed on 9/20/04, as being drawn to a non-elected invention. The Examiner has rejected claims 1-5 and 11-15. Applicant respectfully requests reconsideration of pending claims 1-5 and 11-15.

The Examiner has rejected claims 1-5 and 11-15 under 35 U.S.C. 102(b) as being anticipated by Oki, U.S. Patent No. 5,870,595. Applicant respectfully disagrees.

In section 8 of the Office action, the Examiner states, "In Oki system discloses an activity latch for holding an activity flag value [61, fig. 2; col. 5, lines 8-25]." As Applicant noted in response to the previous Office action, the Examiner appears to have changed the rejection from alleging element 81 of Figure 1 of Oki to disclose an "activity latch" to alleging element 66 of Figure 2 of Oki to disclose an "activity latch." Now, the Examiner cites "[61, fig. 2; col. 5, lines 8-25]" as allegedly disclosing "an activity latch" and "[the size of the available area; col. 5, lines 8-25]" as allegedly disclosing "for holding an activity flag value." Applicant respectfully disagrees.

Regarding claim 1, Applicant submits the cited portion of the cited reference fails to disclose the subject matter set forth in claim 1. For example, Applicant submits the cited portion of the cited reference fails to disclose "an activity latch for holding an activity flag value." While the Examiner alleges "third buffer memory unit" 61 of Oki to disclose "an activity latch" and "[the size of the available area; col. 5, lines 8-25]" to disclose "for holding an activity flag value," Applicant notes that "third buffer memory unit" 61 is depicted as providing only one output, namely reference numeral 72, which is recited as "outgoing data" (col. 5, lines 16 and 17). Applicant can find no teaching in the cited portion of the cited reference that AND circuit 83, which the Examiner alleges as disclosing "a logic element operatively coupled to the activity latch to receive an incoming clock signal and to provide an outgoing clock signal, the outgoing clock signal being dependent on the activity flag value," provides an outgoing clock signal, the outgoing clock signal being dependent on the activity flag value. Moreover, while the Examiner asserts "[the size of the available area]" as allegedly disclosing "an activity flag value," Applicant can find no teaching in the cited portion of the cited reference of "third buffer memory unit 61" holding "the size of the available area" as "an activity flag value." Applicant note the Examiner again cites, "[figures 1 and 2; col. 4, line 58-col. 5, line 29; emphasis added, 'signal

54 is generated based on an value detected by detecting unit 66 from buffer memory 61 (see col. 5, lines 8-12), and output to an AND logic circuit 83 to control an output (clock signal 80) of a clock signal 6 (see fig. 1; col. 5, lines 22-29)']." As Applicant noted in Applicant's response to the previous Office action, Applicant has exhaustively searched the entire Oki reference and is unable to locate such text as purportedly quoted by the Examiner. While the Examiner cites col. 5, lines 8-12, that portion of the cited reference does not appear to contain the text purportedly quoted by the Examiner. Rather, col. 5, lines 8-12, states, "Reference numeral 68 is a comparator which is used for generalizing the second transfer halt signal 54 cited above when the size of the available area in the first buffer memory unit 66 is smaller than a predetermined value." Applicant notes the only mention of "value" in the cited portion of the cited reference is "a predetermined value." Applicant can find no teaching in the cited portion of the cited reference of the "predetermined value" being "an activity flag value" or of "an activity latch for holding" the "predetermined value." Thus, Applicant submits the cited portion of the cited reference fails to anticipate the subject matter set forth in claim 1. Thus, Applicant submits claim 1 is in condition for allowance.

Regarding claim 2, Applicant submits the cited portion of the cited reference fails to disclose the subject matter set forth in claim 2. For example, Applicant submits the cited portion of the cited reference fails to disclose "a second activity flag value held in a second activity latch." As noted above, the Examiner appears to have changed the element the Examiner alleges to disclose "an activity latch" of claim 1 from AND circuit 81 to available-area detecting unit 66 to third buffer memory unit 61 over the last two Office actions. Yet, the Examiner continues to assert AND gates 81a and 81b of Figure 8 of Oki as allegedly disclosing "a second activity latch" of claim 2. Applicant can find no teaching in the cited portion of the cited reference of AND gates 81a or 81b holding a second activity flag value. Moreover, as AND gates are purely combinational logic gates, Applicant submits the AND gates cited by the Examiner fail to disclose a second activity flag value held in a second activity latch. Furthermore, Applicant can find no teaching in the cited portion of the cited reference of "wherein the activity flag value is mutually exclusive with a second activity flag value. Thus, Applicant submits claim 2 is in condition for allowance.

Regarding claim 3, Applicant submits the cited portion of the cited reference fails to disclose the subject matter set forth in claim 3. For example, Applicant submits the cited portion of the cited reference fails to disclose that the logic element passes the incoming clock signal as the outgoing clock signal when the activity flag value has a first value. As Applicant stated with respect claim 1 from

which claim 3 depends, Applicant submits the cited portion of the cited reference fails to disclose "an activity latch for holding an activity flag value." Thus, Applicant submits Oki fails to disclose an "activity flag value" consonant with the subject matter of claim 3. While the Examiner cites col. 5, lines 25-29, and col. 11, lines 34-37, as allegedly disclosing the subject matter of claim 3, Applicant can find no teaching as to "when the activity flag has a first value" in the cited portions of the cited reference. Accordingly, Applicant submits claim 3 is in condition for allowance.

Regarding claim 4, Applicant submits the cited portion of the cited reference fails to disclose the subject matter set forth in claim 4. For example, Applicant submits the cited portion of the cited reference fails to disclose that the logic element blocks the incoming clock signal when the activity flag value has a second value. As Applicant stated with respect claim 1 from which claim 4 depends, Applicant submits the cited portion of the cited reference fails to disclose "an activity latch for holding an activity flag value." Thus, Applicant submits Oki fails to disclose an "activity flag value" consonant with the subject matter of claim 4. While the Examiner cites col. 5, lines 25-29, and col. 11, lines 34-37, as allegedly disclosing the subject matter of claim 4, Applicant can find no teaching as to "when the activity flag has a second value" in the cited portions of the cited reference. Accordingly, Applicant submits claim 4 is in condition for allowance.

Regarding claim 5, Applicant submits the cited portion of the cited reference fails to disclose the subject matter set forth in claim 5. For example, Applicant submits the cited portion of the cited reference fails to disclose that the logic element provides a static output level as the output clock signal when the activity flag value has the second value. As Applicant stated with respect claim 1 from which claim 5 depends, Applicant submits the cited portion of the cited reference fails to disclose "an activity latch for holding an activity flag value." Thus, Applicant submits Oki fails to disclose an "activity flag value" consonant with the subject matter of claim 5. While the Examiner cites col. 5, lines 25-29; col. 11, lines 34-37; col. 11, lines 38-47; and col. 12, lines 14-21, as allegedly disclosing the subject matter of claim 5, Applicant can find no teaching as to "when the activity flag has a second value" in the cited portions of the cited reference. Accordingly, Applicant submits claim 5 is in condition for allowance.

Regarding claims 11-15, the Examiner alleges claims 11-15 are basically the operating step that are carried out by the corresponding elements in claims 1-5 and rejects claims 11-15 for the same reason set forth for claims 1-5. However, Applicant submits claim limitations of claims 1-5 cannot be imputed to claims 11-15, as claims 11-15 do not depend from any of claims 1-5. As to claim 11,

Applicant submits Oki fails to disclose a "first activity latch" as set forth in claim 11. As to claim 12, Applicant submits Oki fails to disclose either a "first activity latch" or a "second activity latch." Moreover, Applicant notes that none of the teachings of Oki, column 11, lines 56-61, cited by the Examiner appear to disclose the feature of claim 12 "the second activity flag value being mutually exclusive of the first activity flag value." Thus, Applicant submits that claim 12 is in condition for allowance. Regarding claims 13-15, as noted above, Applicant submits Oki fails to disclose the features of claim 11 from which claims 13-15 depend. Moreover, Applicant submits Oki fails to disclose a "first activity flag value" consonant with the subject matter of claims 13-15. Thus, Applicant submits claims 13-15 are in condition for allowance.

The Examiner has rejected claims 1, 3-5, 11, and 13-15 under 35 U.S.C. 102(b) as being anticipated by Karibe et al., JP Patent No. 64-48142. Applicant respectfully disagrees.

In section 8 of the Office action, the Examiner states, "Karibe discloses an activity latch of a line card [fig. 2] for holding an activity flag value [counter 5; abstract all]." Applicant respectfully disagrees. Besides that sentence in section 8 of the present Office action, it appears to Applicant that the Examiner has copied verbatim the entire text of the rejections based on the Karibe reference from the previous Office action. Applicant has previously presented arguments for the allowability of claims 1, 3-5, 11, and 13-15 over the Karibe reference. Applicant reiterates Applicant's previously presented arguments.

Regarding claims 1, 3, and 4, Applicant reiterates Applicant's previously presented arguments. Applicant submits claims 1, 3, and 4 are in condition for allowance.

Regarding claim 5, the Examiner repeats verbatim the same rejection made in the previous Office action. As Applicant stated in response to the previous Office action, the Examiner appears not to have complied with MPEP 2112 or existing law in asserting a rejection based on inherency. Thus, Applicant submits the subject matter recited in claim 5 cannot be considered to be inherent in the teachings of the cited reference. Therefore, Applicant submits the Examiner has not shown claim 5 to be anticipated by the cited reference. Consequently, Applicant submits claim 5 is in condition for allowance.

Regarding claims 11 and 13-15, the Examiner states, "As to claims 11-15 basically are the operating step that are carried out by the corresponding elements in claims 1-5." Accordingly, claims 11-15 are rejected for the same reason as set forth for claims 1-5." However, Applicant submits claim

limitations of claims 1-5 cannot be imputed to claims 11-15, as claims 11-15 do not depend from any of claims 1-5. Regarding claim 11, Applicant can find no teaching in the cited portion of the cited reference of "...a first activity latch of a first line card of the plurality of line cards." Regarding claim 13-15, as Applicant has presented arguments that the cited portion of the cited reference fails to disclose the features of claim 11, from which claims 13-15 depend, Applicant submits the cited portion of the cited reference fails to disclose features consonant with the subject matter recited in claims 13-15. Thus, Applicant submits claims 11 and 13-15 are in condition for allowance.

The Examiner has rejected claims 1 and 11 under 35 U.S.C. 102(b) as being anticipated by Senoh, U.S. Patent No. 5,914,580. Applicant respectfully disagrees.

Applicant notes that, in the previous Office action, the Examiner stated the following regarding the Senoh reference: "8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Senoh, US patent no. 5,914,580, discloses a circuit having an activity latch for holding an activity flag value, and controlling an output of a clock signal base on the activity flag value [fig. 2; col. 5, lines 19-26]." Applicant further notes the Examiner did not base any rejections on the Senoh reference in the previous Office action. Now, in this Office action, the Examiner bases a 102(b) rejection on the same portions of the Senoh reference cited in the previous Office action.

Regarding claim 1, Applicant submits the cited portions of the cited reference fail to disclose the subject matter set forth in claim 1. For example, Applicant submits the cited portion of the cited reference fails to disclose "an activity latch for holding an activity flag value." While the Examiner cites "[10, fig. 2]" and "[col. 4, lines 45-53]," Applicant can find no teaching in the cited portions of the cited reference of "an activity latch for holding an activity flag value." Also, Applicant notes the subject matter of claim 1 is directed to a "line card circuit." Applicant can find no teaching in the cited portion of the cited reference of a "line card circuit." Thus, Applicant submits claim 1 is in condition for allowance.

Regarding claim 11, Applicant submits the cited portions of the cited reference fail to disclose the subject matter set forth in claim 11. For example, Applicant submits the cited portion of the cited reference fails to disclose "receiving a first activity flag value from a first activity latch of a first line card circuit of the plurality of line card circuits." The Examiner states "claim 11 is rejected for the same reasons as set forth for claim 1." For the rejection of claim 1, the Examiner cites "[10, fig. 2]" and "[col. 4, lines 45-53]." Applicant can find no teaching in the cited portions of the cited reference

of "...a first activity latch of a first line card of the plurality of line cards." Applicant submits the cited reference appears to be directed to a drive control device for a stepping motor, not a first line card circuit of a plurality of line card circuits. Thus, Applicant submits claim 11 is in condition for allowance.

In conclusion, Applicant has overcome all of the Office's rejections, and early notice of allowance to this effect is earnestly solicited. If, for any reason, the Office is unable to allow the Application on the next Office Action, and believes a telephone interview would be helpful, the Examiner is respectfully requested to contact the undersigned attorney.

Respectfully submitted,

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Date

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